IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Toshiyuki Matsuzaki	Docket:	TIJ-29142
Serial No.	TBD	Examiner:	Not Assigned
Filed:	12/20/2000	Art Unit:	TBD
For:	Source Driver		

PRELIMINARY AMENDMENT

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

'EXPRESS MAIL" mailing label number **EL360245091US.** Date of Deposit: **20 December 2000.** I hereby certify that the accompanying Application is being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the above-mentioned date and addressed to the Assistant Commissioner of Patents, Washington, D C 20231.

Allen B. Kroger — Date 12/20/00

Assistant Commissioner For Patents

Washington, D. C. 20231

Sir:

Please amend the above-referenced application as follows:

In the Specification:

Page 3 before line 10, add --SUMMARY OF THE INVENTION--

line 10, delete "The purpose" and substitute therefor --A general object--

line 14, delete "In order to achieve said purpose, this invention's" and substitute therefor --This and other objects and features are attained, in accordance with one aspect of the invention by a--

line 14, delete "has" and substitute therefor --having--

Page 4 line 16, delete "SUMMARY OF THE INVENTION" through page 5 line 23 "and said first terminal in said signal terminals of adjacent sets."

Page 5 line 24, delete "[Effects of the invention] With the" and substitute therefor --The--

line 24, delete "this" and substitute therefor --one--

line 24, delete ", by providing" and substitute therefor --provides--

In the Claims:

The claims appearing in the specification at page 4, line 17 through page 5, line 23 are inserted at the end of the specification on separate sheets as follows:

[[Claim 1]] Claim 1. (Amended) A module for a display device that has a semiconductor chip that has n (where n is a natural number and n>=2) signal input terminals as well as n input terminals and n output terminals to be connected respectively to said n signal input terminals, and includes a switching circuit that sequentially connects said first through n-th input terminals to said first through n-th output terminals respectively when a control signal is at the first logical level and sequentially connects said first through n-th input terminals to said n-th through first output terminals respectively when said control signal is at the second logical level, a drive signal generation circuit that generates drive signals that drive a display device based on image signals output from the output terminals of said switching circuit, and m (where m is a natural number and m>=2) signal output terminals for outputting said drive signals, a first substrate that includes n input terminals and n first lines that connect said input terminals and the signal input terminals of said semiconductor chip respectively, and m output terminals and m second lines that connect said output terminals and the signal output terminals of said semiconductor chip respectively, and on which said semiconductor chip is mounted, and a second substrate that includes n sets of signal terminals that correspond respectively to the n input terminals of said first substrate and n sets of lines that sequentially connect the first through n-th signal terminals of the N-th (where N is a natural number and 1<=N<=n-1) set to the n-th through first signal terminals of the (N+1)-th set respectively, and by which said n signal terminals are connected to the n input terminals of said first substrate.

[[Claim 2]] Claim 2. (Amended) A module for a display device as described in claim 1 [in which] wherein the logical level of the control signals supplied to semiconductor chip arranged corresponding to odd numbers and the logical level of the control signals supplied

to semiconductor chips arranged corresponding to even numbers are the reverse of each other.

[[Claim 3]] Claim 3. (Amended) A module for a display device as described in claim 2 [in which] wherein the n sets of signal terminals of said second substrate are arranged linearly approximately in a row, and the m output terminals of said first substrate are connected to the signal electrodes of a liquid-crystal display.

[[Claim 4]] Claim 4. (Amended) A module for a display device as described in claim 1[, 2, or 3 in which] wherein said first substrate is a flexible substrate.

[[Claim 5]] Claim 5. (Amended) A module for a display device as described in claim 1[, 2, 3, or 4 in which] wherein the input terminals of said first substrate and the signal terminals of the second substrate include a first terminal and second terminal respectively, the first line of said first substrate includes a first wiring part that connects said first terminal and the signal input terminal of said semiconductor chip and a second wiring part that connects said second terminal and the signal input terminal of said semiconductor chip, and the wiring of said second substrate connects said second terminal and said first terminal in said signal terminals of adjacent sets.

Please add claims 6-10 as follows:

--Claim 6. A module for a display device as described in claim 2 wherein said first substrate is a flexible substrate.

Claim 7. A module for a display device as described in claim 3 wherein said first substrate is a flexible substrate.

Claim 8. A module for a display device as described in claim 2 wherein the input terminals of said first substrate and the signal terminals of the second substrate include a first terminal and second terminal respectively, the first line of said first substrate includes a first wiring part that connects said first terminal and the signal input terminal of said semiconductor chip and a second wiring part that connects said second terminal and the signal input terminal of said semiconductor chip, and the wiring of said second substrate connects said second terminal and said first terminal in said signal terminals of adjacent sets.

Claim 9. A module for a display device as described in claim 3 wherein the input terminals of said first substrate and the signal terminals of the second substrate include a first terminal and second terminal respectively, the first line of said first substrate includes a first wiring part that connects said first terminal and the signal input terminal of said semiconductor chip and a second wiring part that connects said second terminal and the signal input terminal of said semiconductor chip, and the wiring of said second substrate connects said second terminal and said first terminal in said signal terminals of adjacent sets.

Claim 10. A module for a display device as described in claim 4 wherein the input terminals of said first substrate and the signal terminals of the second substrate include a first terminal and second terminal respectively, the first line of said first substrate includes a first wiring part that connects said first terminal and the signal input terminal of said semiconductor chip and a second wiring part that connects said second terminal and the signal input terminal of said semiconductor chip, and the wiring of said second substrate connects said second terminal and said first terminal in said signal terminals of adjacent sets.--

IN THE DRAWINGS

A proposed drawing correction is enclosed herewith.

REMARKS

The application and claims have been amended to place them in the appropriate form and to eliminate multiple claim dependencies. Early action on the merits is earnestly requested.

Respectfully submitted,

William B. Kempler
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SUBMISSION OF PROPOSED DRAWING AMENDMENT FOR APPROVAL BY EXAMINER (37 C.F.R. § 1.123

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Allen B. Kroger — Date: 12/20/00

Assistant Commissioner For Patents
Washington, DC 20231
Attention: Official Drafts Person

Dear Sir:

Attached please find

[ ] a sketch in permanent ink,

[**X**] a copy of the original drawing(s) with red ink markings,

showing the proposed changes to the drawing(s) in the application, for which the approval of the Examiner is requested.

Respectfully submitted,

William B. Kempler
Senior Corporate Patent Counsel
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整理番号＝９９０５１５ (1)

【書類名】 図面

【図１】

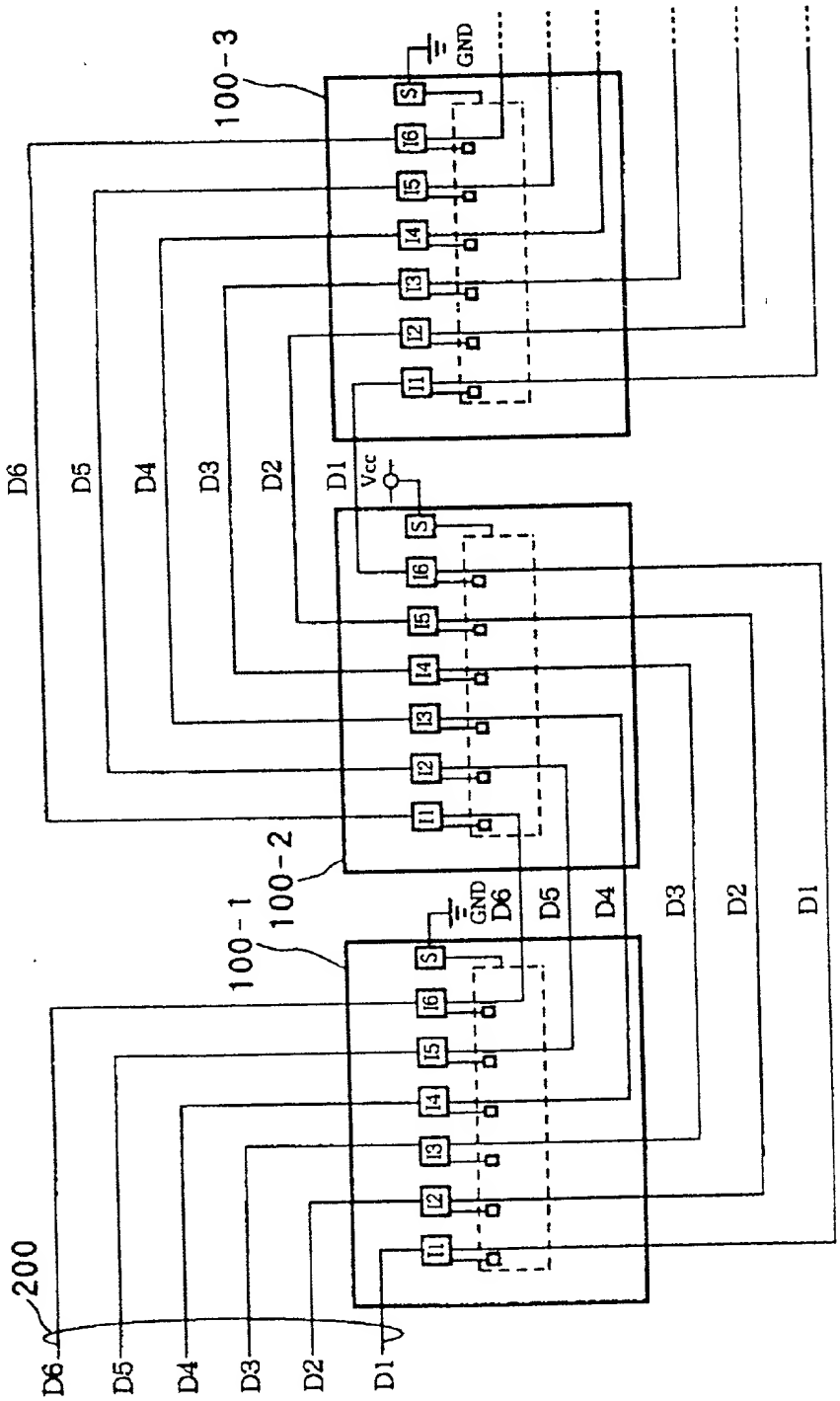
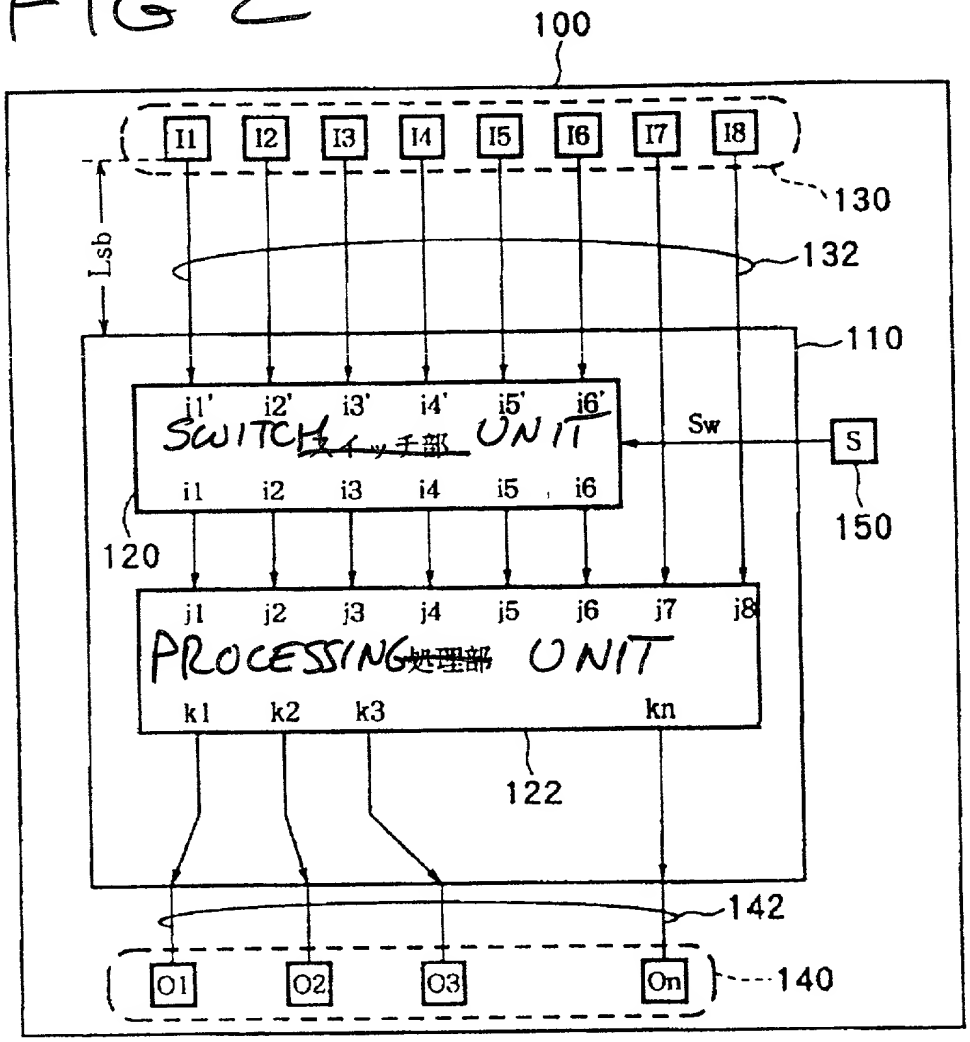


FIG. 1

整理番号＝９９０５１５ (2)

【図２】

FIG 2



【図３】

Sw	INPUT	i1'	i2'	i3'	i4'	i5'	i6'
L	OUTPUT	i1	i2	i3	i4	i5	i6
H		i6	i5	i4	i3	i2	i1

FIG 3

整理番号＝９９０５１５ (3)

【図４】

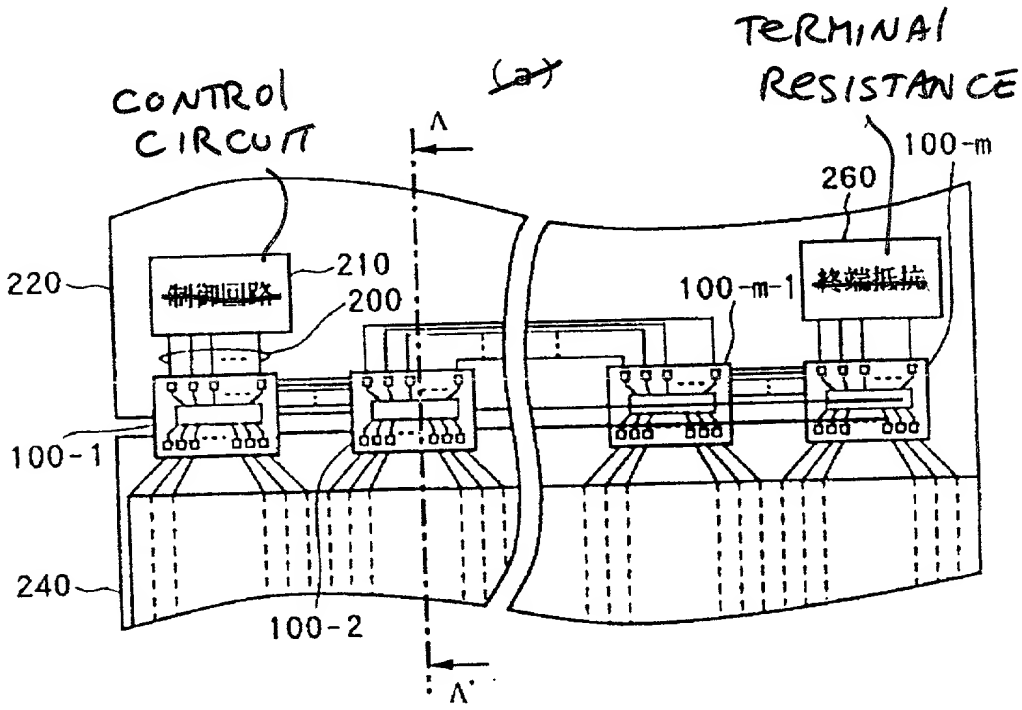


FIG 4A

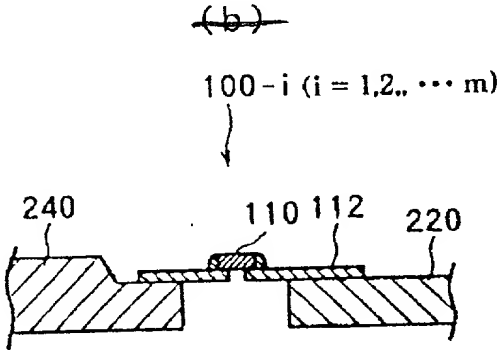


FIG 4B

整理番号＝'９９０５１５ (4)

【図５】

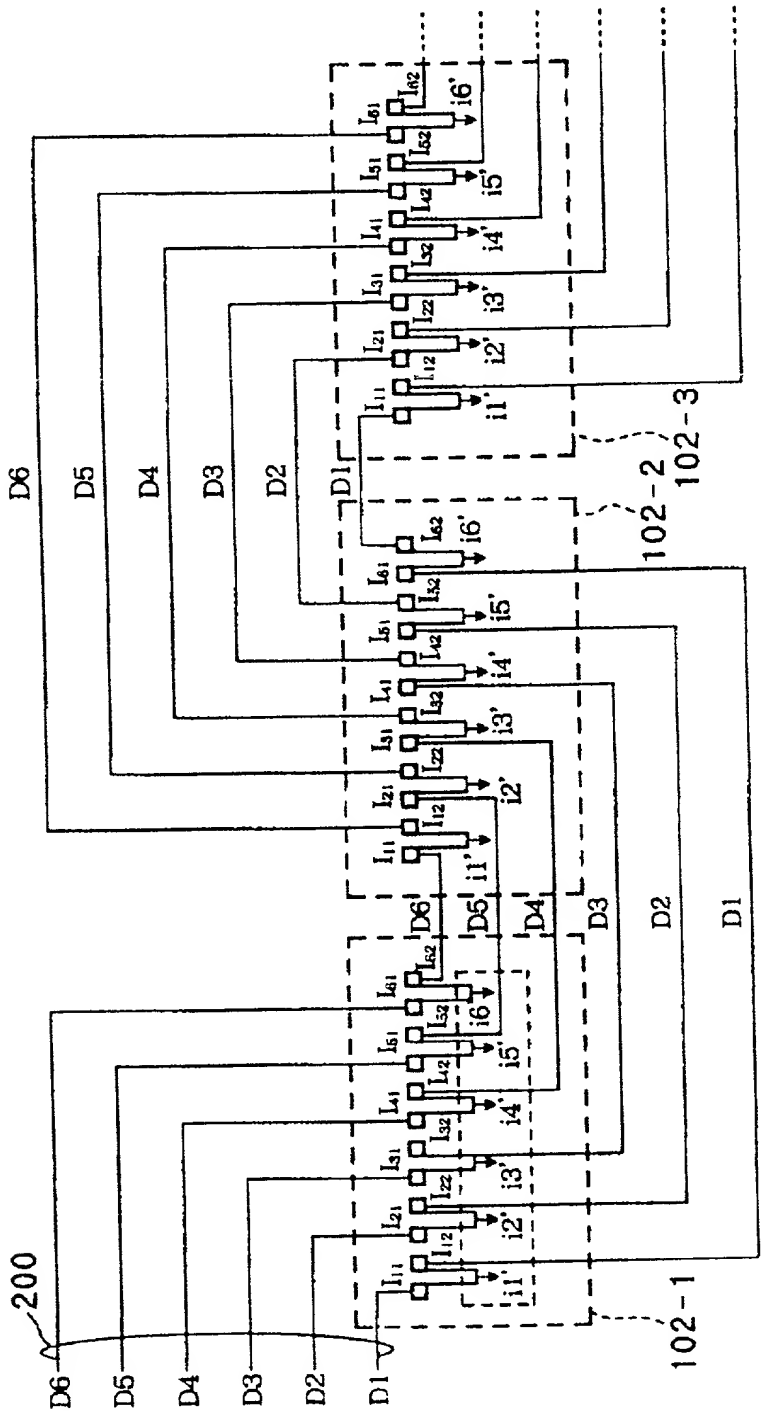


FIG. 5

整理番号 990 15 (5)

【図6】

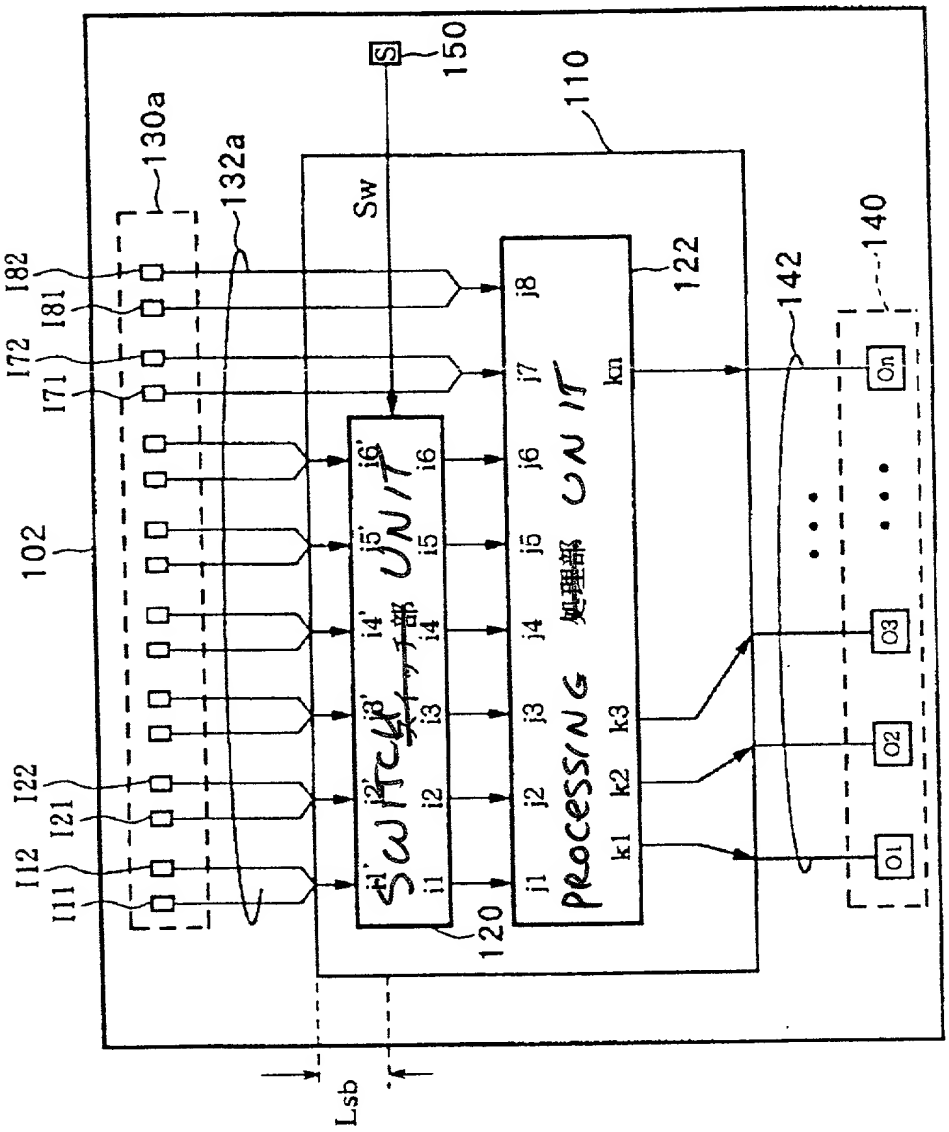


FIG. 6

【図7】

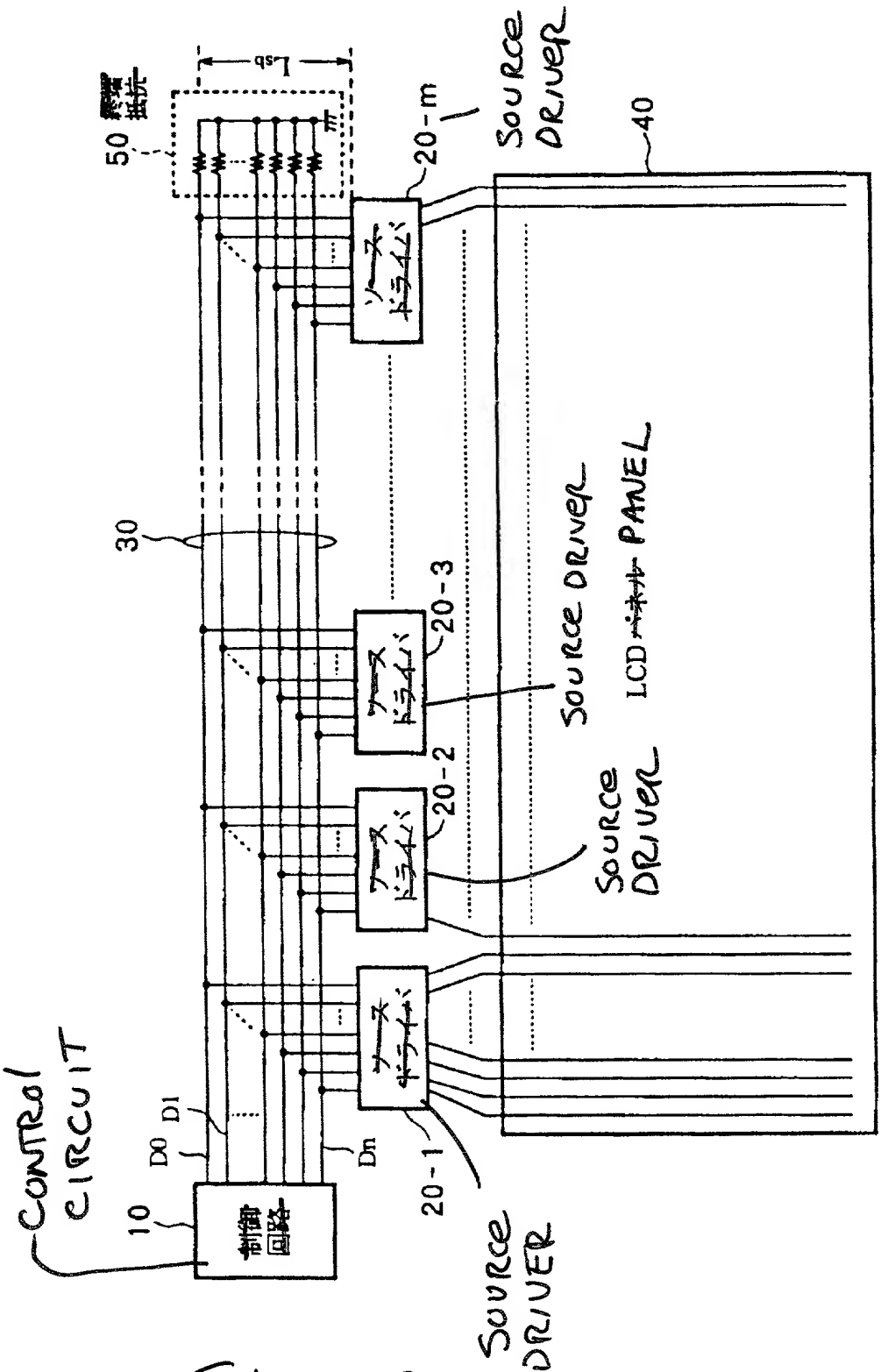

50
30
10
CONTROL CIRCUIT
D0
D1
Dn
20-1
20-2
20-3
20-m
SOURCE DRIVER
SOURCE DRIVER
SOURCE DRIVER
SOURCE DRIVER
40
LCD PANEL

FIG. 7

整理番号='９９０５１５ (7)

【図８】

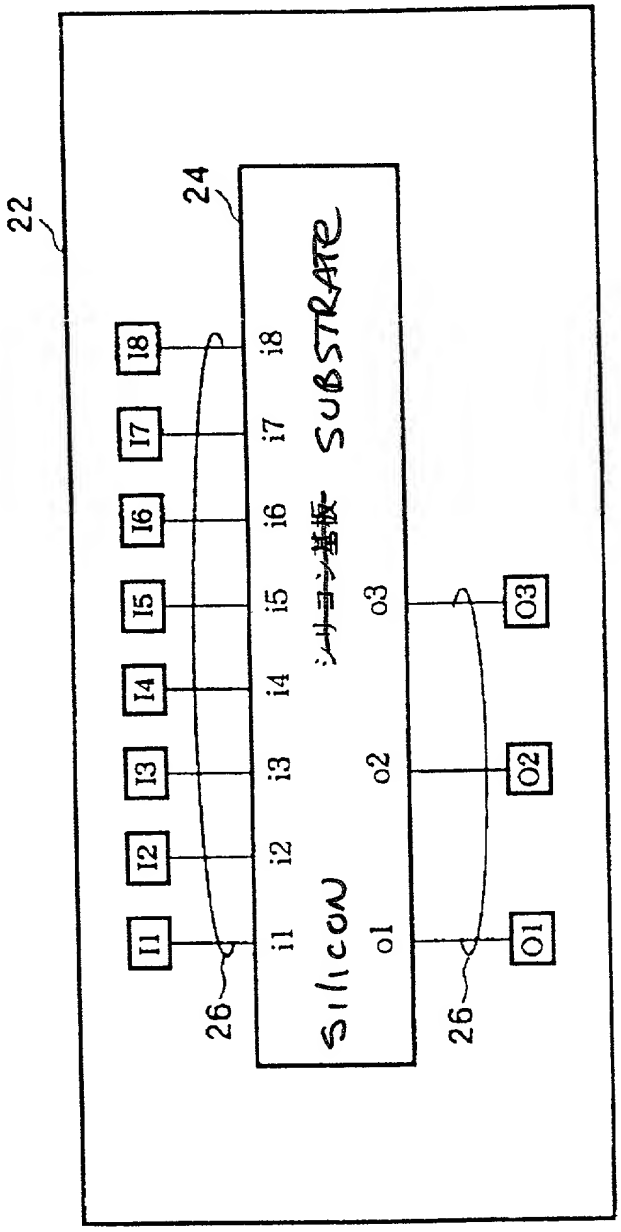


FIG. 8

整理番号＝９９０　１５　(8)

【図９】

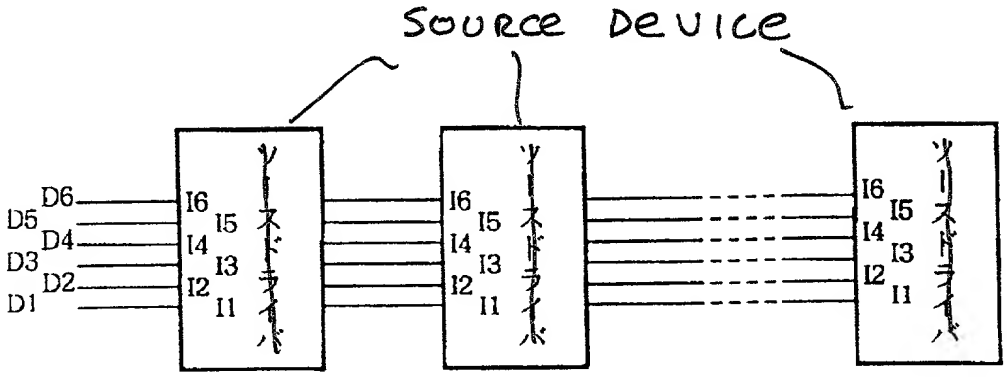


FIG. 9